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Presented for filing is a new original patent application of:

Applicant: JAMES A. McCALL, RANDY M. BONELLA, JOHN B. HALBERT, JIM M. DODD AND CHUNG LAM

Title: BUFFERING DATA TRANSFER BETWEEN A CHIPSET AND MEMORY MODULES

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Enclosed are the following papers, including those required to receive a filing date under 37 CFR 1.53(b):

	Pages
Specification	8
Claims	6
Abstract	1
Declaration	[To be Filed at a Later Date]
Drawing(s)	5

Enclosures:
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Basic filing fee	$0
Total claims in excess of 20 times $18	$0
Independent claims in excess of 3 times $78	$0
Fee for multiple dependent claims	$0
Total filing fee:	$0

Under 37 CFR §1.53(f), no filing fee is being paid at this time.

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Respectfully submitted,

Reg No. 42791

for Scott C. Harris
Reg. No. 32,030
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Attorney's Docket No.: 10559/348001 / P9836

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: BUFFERING DATA TRANSFER BETWEEN A CHIPSET AND MEMORY MODULES

APPLICANT: JAMES A. McCALL, RANDY M. BONELLA, JOHN B. HALBERT, JIM M. DODD AND CHUNG LAM

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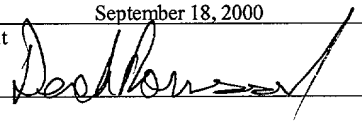
Signature

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BUFFERING DATA TRANSFER BETWEEN A CHIPSET AND MEMORY MODULES

BACKGROUND

The present disclosure relates to providing data buffers in an interface between a chipset and memory modules.

Computer systems often contain one or more integrated circuit (IC) chips that are coupled to memory modules using a memory interface. These IC chips may be controllers referred to as chipsets. The memory interface provides communication between the IC chipset (e.g. the CPU) and the memory modules. The memory interface may contain address bus lines, command signal lines, and data bus lines. Increasing demand for higher computer performance and capacity has resulted in a demand for a larger and faster memory. However, as the operating speed and the number of memory modules connected to the chipset increase, the increased capacitive loading may place substantial limit on the amount and speed of memory.

Prior art designs, such as a registered dual in-line memory module (DIMM), have addressed the above-described difficulties by providing an address/command buffer in the address bus lines and the command signal lines to relieve the capacitive loading effects. Karabatsos (U.S. Patent No.

5,953,215) describes a loading relief design for the data bus lines by providing FET switches in the interface between the chipset and the memory modules.

BRIEF DESCRIPTION OF THE DRAWINGS

Different aspects of the disclosure will be described in reference to the accompanying drawings wherein:

FIG. 1 shows a prior art design of an interface between a chipset and memory modules;

FIG. 2 illustrates an embodiment of an interface having a plurality of data buffers disposed between the chipset and the memory modules;

FIG. 3 shows a layout configuration of a data buffer;

FIG. 4 is a front view of the interface showing the details of memory boards having the memory modules; and

FIG. 5 shows a process for buffering the data passed between the chipset and the memory modules.

DETAILED DESCRIPTION

The inventors of the present disclosure recognized that none of the prior art designs offer isolation of supply voltages and interfaces coupled to the chipset and the memory modules. Buffering the address and command lines relieves the capacitive loading effects, while providing the

FET switches in the data lines offers a loading relief on those lines. However, neither design provides electrical isolation between the chipset and the memory data.

The differences in fabrication process between the chipset and the memory modules place additional burdens on the computer system design. For example, oxides on a memory chip are designed to be thick to provide capacitors with good retention characteristic. Thick oxides also keep leakage current low. However, a higher voltage (on the order of about 1.2 to 1.8 volts) must be supplied to build conducting channels beneath the oxides. The Central Processing Unit (CPU) or application-specific integrated circuit (ASIC) design fabrication process on the chipset side, on the other hand, promotes thinner oxides providing faster transistors. Therefore, the chipset may be operated at a lower voltage, typically less than 1.0 volt.

The present disclosure describes methods and systems for buffering data transfer between a chipset and memory modules. The method includes providing and configuring at least one buffer provided in an interface between a chipset and memory modules. The buffer allows the interface to be split into first and second sub-interfaces. The first sub-interface is between the chipset and the buffer. The second sub-interface is between the buffer and the memory modules. The buffer is configured to latch the data being transferred

between the chipset and the memory modules. The first and second sub-interfaces operate independently but synchronized with each other.

Buffering provides isolation of voltages and interfaces coupled to each of the chipset and the memory modules. The isolation of voltages allows the chipset to be operated with only a low operating voltage, which substantially precludes the need for the chipset to have a higher voltage common with a memory supply voltage. The memory module is then allowed to operate at voltages appropriate for its own operational purpose. The voltages may be independent of the operating voltage at the connecting system (chipset).

The isolation of the interfaces allows the inherently faster chipset interface to run at higher multiples of the memory interface rate. For example, the chipset to data buffer interface may run at twice the rate of the buffer to memory interface. This may allow the chipset to operate at twice the rate and access the same amount of data with half the number of data bus lines or pins. This provides computer system designers with a flexibility of utilizing a wider range of memory types and interfaces for a particular computer system. Further, by providing a data buffer on the memory module itself, the memory interface may be simplified by providing a short, fixed length stubs from the buffer to the memory module. In some configurations, the data buffer

may be provided on the same motherboard as the chipset. An advantage provided by the electrical isolation that leads to the reduction in the number of pin count is illustrated in the design comparison between FIGS. 1 and 2.

In the prior art design 100 of FIG. 1, the interface 108 between the chipset 102 and the memory modules 104 is unbuffered. In some embodiments, the memory modules 104 may be individually mounted on memory boards 106 as shown. In other embodiments, the memory modules 104 may be soldered directly onto the same motherboard as the chipset 102.

In the prior art design 100, the chipset 102 is configured to receive two supply voltages, 1.0 volt (low) and 1.5 volts (high). The high voltage is necessary on the chipset side to provide compatible driving voltage on the memory interface 108. Further, the pin count on the chipset 102 may be designed to be *2x* in order to provide a particular memory access rate or frequency, such as ω.

In the illustrated embodiment 200 of FIG. 2, a plurality of data buffers 206 are disposed in the memory interface between the chipset 202 and the memory modules 204 to provide electrical isolation. For the illustrated embodiment, a multidrop bus 208 provides the interface between the chipset 202 and the data buffers 206. The interface between the chipset 202 and the data buffers 206

may be run at the same data access rate or frequency (ω) as before, but with half the pin count (x) of the prior art design. The interface between the data buffers 206 and the memory modules 204 still has $2x$ number of pins to provide the same data access rate as before. In practice, x is often selected to be 16 or 32. Moreover, the chipset 202 is configured to operate with only the low voltage (1.0 volt) as shown. The memory modules 204 are operated with only the high voltage (1.5 volts).

In the illustrated embodiment of FIG. 2, the data buffer 206 is provided on the same memory board 210 as the memory module 204. However, the data buffer 206 may be provided on the motherboard containing the chipset 202.

FIG. 3 shows a layout configuration of a data buffer 300, similar to the data buffer 206 of FIG. 2, in accordance with an embodiment of the present disclosure. The data buffer 300 includes three portions 302, 304, 306. The first portion 302 is a chipset input/output (I/O) port configured to send and receive data to and from the chipset through the multidrop bus 208. The first portion 302 operates at the same voltage (< 1.0 volts) as the chipset. This allows compatibility of interface between the chipset and the data buffer 300. The second portion 304 is a core data path logic portion allowing for buffering of data between the

chipset and the memory module. The third portion 306 is a memory I/O port configured to send and receive data to and from the memory module. The third portion 306 operates at the same nominal voltage as the memory module (between 1.2 and 1.8 volts).

FIG. 4 is a front view of the memory interface showing the details of the memory boards 402, and highlighting the connections to the data buffers 404. The front view of the memory interface shows the isolation of the memory modules 406 from the chipset 408. With separation of the address and data bus lines shown, the reduction in the pin count can be ascertained. The memory modules in this and other embodiments may be of any memory types. However, in particular, the memory modules may be dynamic random access memories (DRAM), double data rate (DDR) DRAM, or quad data rate (QDR) DRAM. The quad data rate DRAM may be achieved by providing a pin count of *4x* in the second sub-interface between the buffer and the memory module, and operating the first sub-interface between the buffer and the chipset at 4 times the rate of the second sub-interface (see FIG. 2).

FIG. 5 shows a process for buffering the data passed between the chipset and the memory modules to provide isolation of voltages and interfaces. The method includes providing at least one buffer in an interface between a

chipset and memory modules at 500. The buffers allow the memory interface to be split into two interfaces. The first interface is between the chipset and the buffers. The second interface is between the buffers and the memory modules. The at least one buffer is then configured to properly latch the data at 502. This allows the first and second interfaces to operate independently but in sync with each other.

While specific embodiments of the invention have been illustrated and described, other embodiments and variations are possible. For example, although the figures show data buffers providing double (i.e. factor = 2) the memory data access rate for a particular number of pin counts, the factor may be any feasible number that affords increased data access rate.

All these are intended to be encompassed by the following claims.

What is claimed is:

1. A method, comprising:

providing at least one buffer in an interface between a chipset and memory modules, said at least one buffer allowing the interface to be split into first and second sub-interfaces, where the first sub-interface is between the chipset and the at least one buffer, and the second sub-interface is between the at least one buffer and the memory modules; and

configuring said at least one buffer to properly latch the data being transferred between the chipset and the memory modules, such that the first and second sub-interfaces operate independently but in synchronization with each other.

2. The method of claim 1, wherein said providing said at least one buffer isolates the first and second sub-interfaces in such a manner that the first sub-interface is operated at different voltage level than the second sub-interface.

3. The method of claim 2, wherein an operating voltage level of said first sub-interface is less than 1.0 volt.

4. The method of claim 2, wherein an operating voltage level of said second sub-interface is between 1.2 and 1.8 volts.

5. The method of claim 1, wherein said providing said at least one buffer isolates the first and second sub-interfaces in such a manner that the first sub-interface is operated at higher frequency than the second sub-interface.

6. The method of claim 5, wherein said first sub-interface is operated at twice the frequency of the second sub-interface.

7. The method of claim 6, wherein a number of data lines in said first sub-interface is half that of a number of data lines in said second sub-interface.

8. The method of claim 1, wherein said at least one buffer are provided on a same memory board as the memory modules corresponding to said at least one buffer.

9. The method of claim 1, wherein said chipset is provided on a motherboard.

10. The method of claim 1, wherein said interface between the chipset and the memory modules is a multidrop bus.

11. The method of claim 1, wherein each of said memory modules includes dynamic random access memory (DRAM).

12. The method of claim 1, wherein each of said memory modules includes double data rate (DDR) DRAM.

13. The method of claim 1, wherein each of said memory modules includes quad data rate (QDR) DRAM.

14. A method, comprising:

providing at least one buffer in an interface between a chipset and memory modules, said at least one buffer allowing the interface to be split into first and second sub-interfaces, where the first sub-interface is between the chipset and the at least one buffer, and the second sub-interface is between the at least one buffer and the memory modules, said at least one buffer isolates the first and second sub-interfaces in such a manner that the first sub-interface is operated at different voltage level than the second sub-interface, and the first sub-interface is operated at higher frequency than the second sub-interface; and

configuring said at least one buffer to properly latch the data being transferred between the chipset and the memory modules, such that the first and second sub-interfaces operate independently but in synchronization with each other.

15. The method of claim 14, wherein said providing said at least one buffer isolates the first and second sub-interfaces in such a manner that the first sub-interface is operated at different voltage level than the second sub-interface.

16. The method of claim 14, wherein said providing said at least one buffer isolates the first and second sub-interfaces in such a manner that the first sub-interface is operated at higher frequency than the second sub-interface.

17. A method, comprising:

isolating a memory interface between a chipset and memory modules, where said isolating divides the memory interface into first and second sub-interfaces; and

configuring said first and second sub-interfaces to properly transfer data between the chipset and the memory modules, such that the first and second sub-interfaces operate independently but in synchronization with each other,

wherein said first and second sub-interfaces are configured in such a manner that the first sub-interface is operated at different voltage level and at higher frequency than the second sub-interface.

18. The method of claim 17, wherein an operating voltage level of said first sub-interface is less than 1.0 volt, and an operating voltage level of said second sub-interface is between 1.2 and 1.8 volts.

19. The method of claim 17, wherein said first sub-interface is operated at twice the frequency of the second sub-interface, and a number of data lines in said first sub-interface is half that of a number of data lines in said second sub-interface.

20. A system, comprising:

a memory interface between a chipset and at least one memory module; and

at least one buffer disposed in said memory interface to divide said memory interface into first and second sub-interfaces,

where said first and second sub-interfaces are configured in such a manner that the first sub-interface is operated at different voltage level and at higher frequency than the second sub-interface.

21. The system of claim 20, wherein an operating voltage level of said first sub-interface is less than 1.0 volt, and an operating voltage level of said second sub-interface is between 1.2 and 1.8 volts.

22. The system of claim 20, wherein said first sub-interface is operated at twice the frequency of the second sub-interface.

23. The system of claim 22, wherein a number of data lines in said first sub-interface is half that of a number of data lines in said second sub-interface.

ABSTRACT

Buffering data transfer between a chipset and memory modules is disclosed. The disclosure includes providing and configuring at least one buffer. The buffers are provided in an interface between a chipset and memory modules. The buffers allow the interface to be split into first and second sub-interfaces. The first sub-interface is between the chipset and the at least one buffer. The second sub-interface is between the at least one buffer and the memory modules. The buffers are then configured to properly latch the data being transferred between the chipset and the memory modules. The first and second sub-interfaces operate independently but in synchronization with each other.

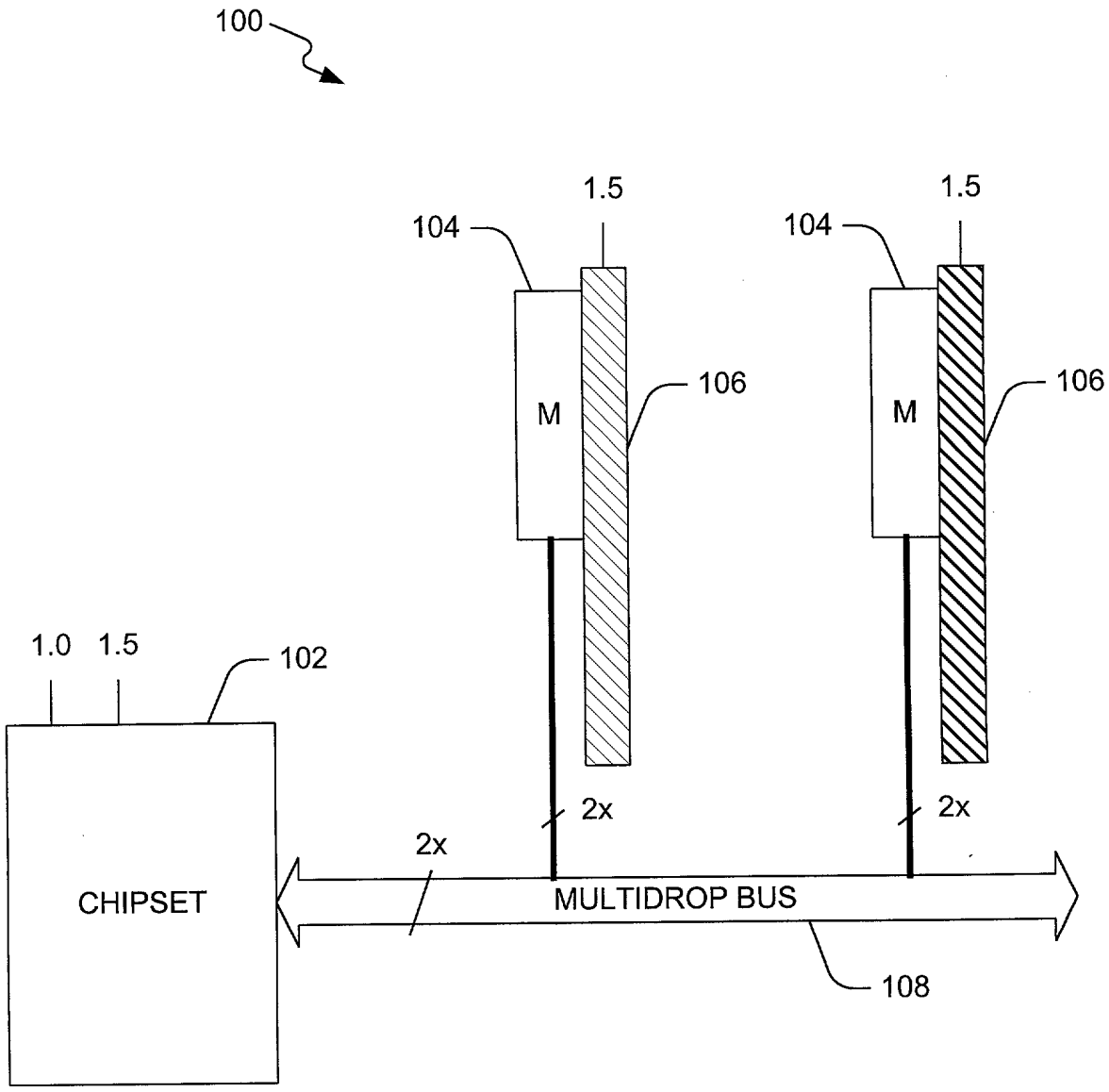


FIG. 1
(PRIOR ART)

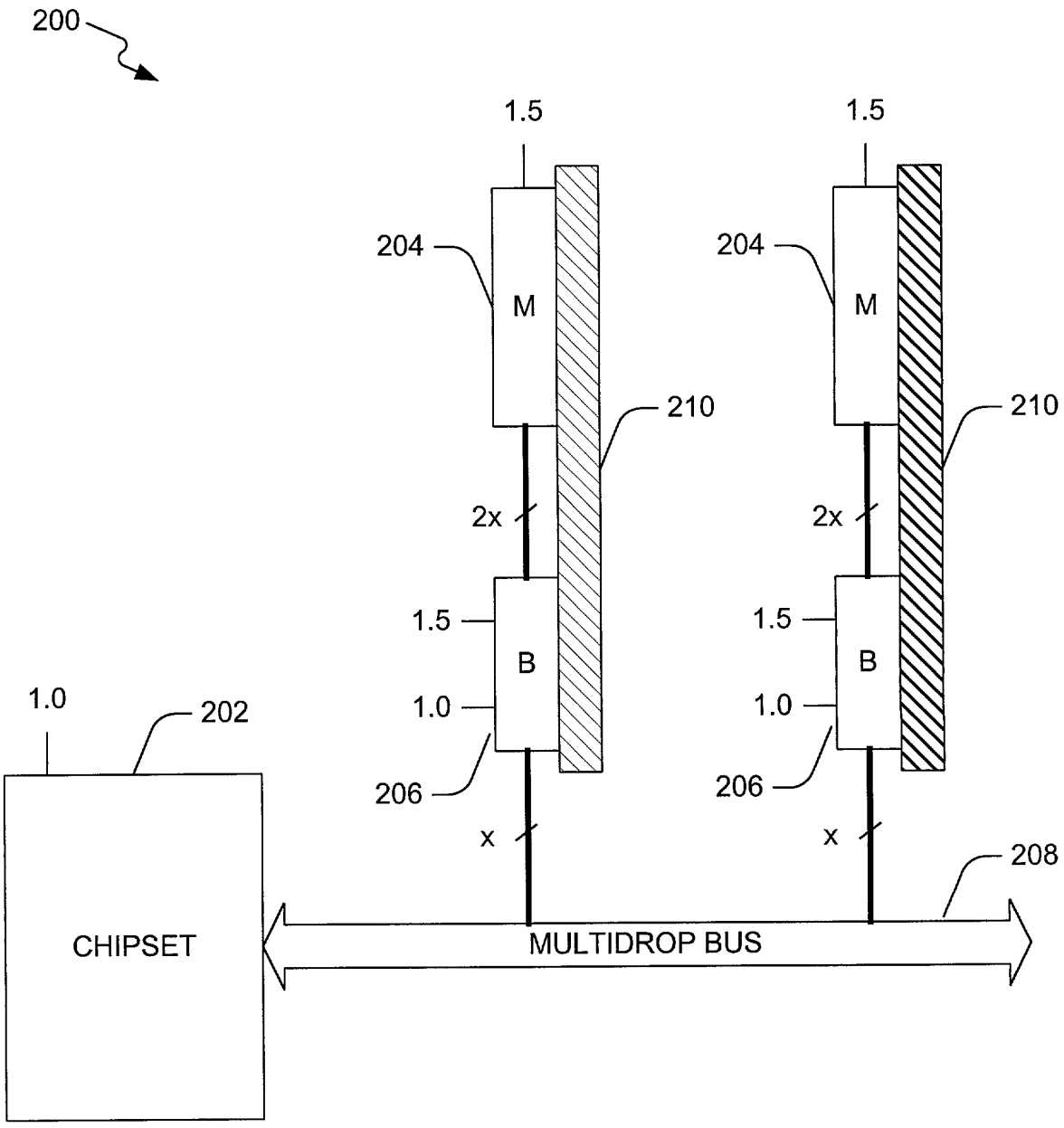

200
1.5
1.5
204
M
204
M
210
210
2x
2x
1.5
B
1.5
B
1.0
1.0
206
206
x
x
208
1.0
202
CHIPSET
MULTIDROP BUS

FIG. 2

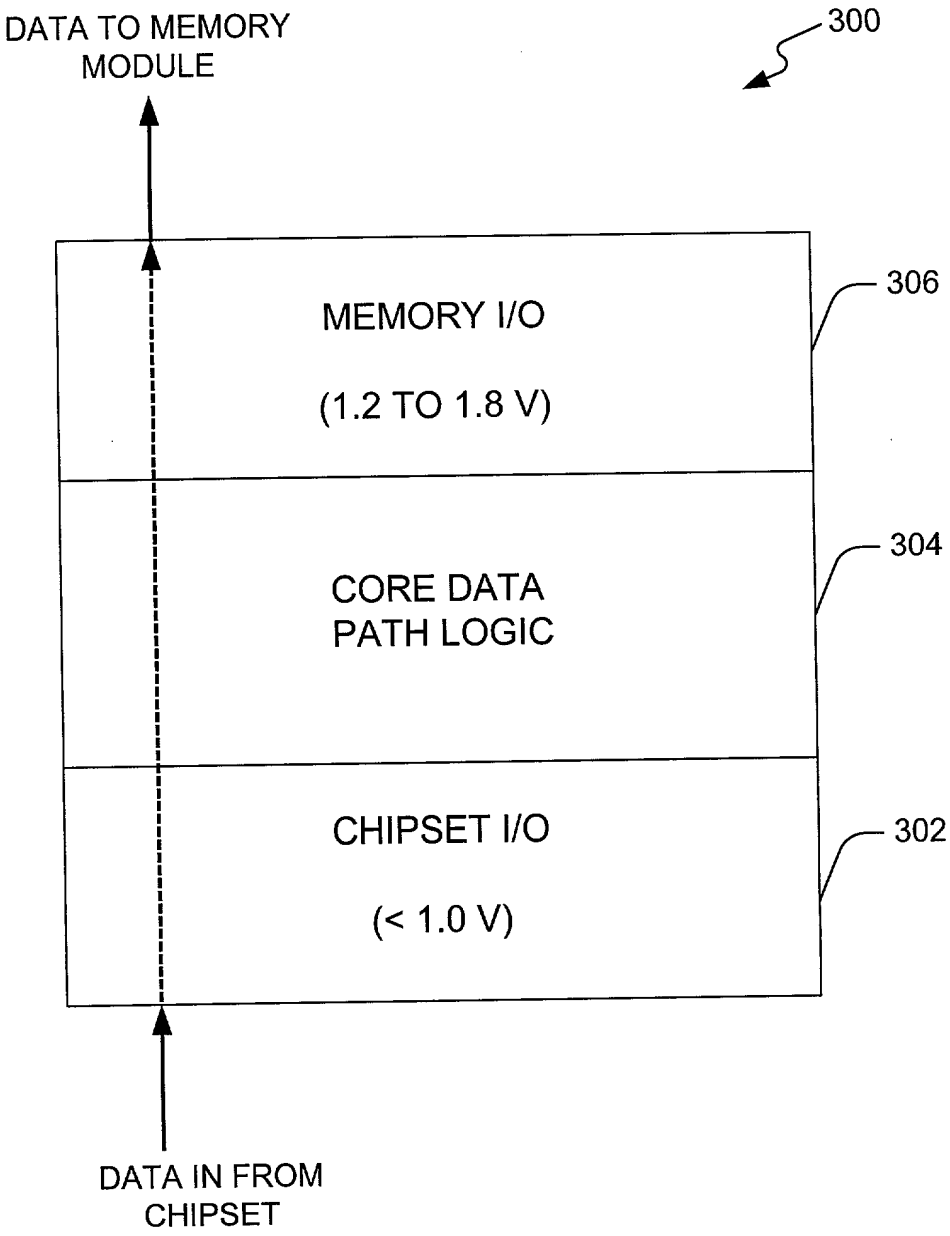
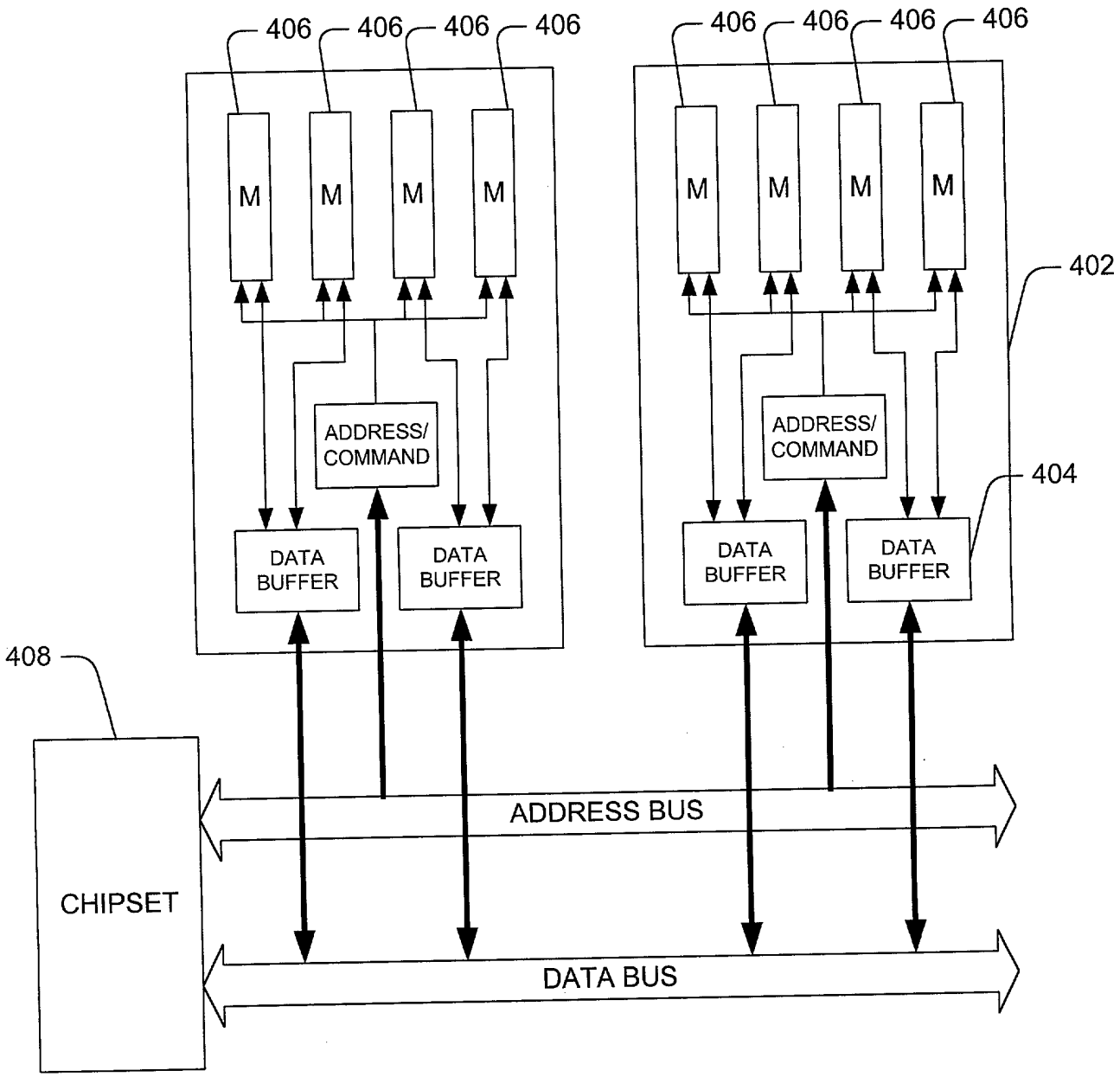

DATA TO MEMORY MODULE
300
MEMORY I/O
(1.2 TO 1.8 V)
306
CORE DATA PATH LOGIC
304
CHIPSET I/O
(< 1.0 V)
302
DATA IN FROM CHIPSET

FIG. 3


406
406
406
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M
M
M
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M
M
M
M
402
ADDRESS/
COMMAND
ADDRESS/
COMMAND
404
DATA
BUFFER
DATA
BUFFER
DATA
BUFFER
DATA
BUFFER
408
CHIPSET
ADDRESS BUS
DATA BUS

FIG. 4

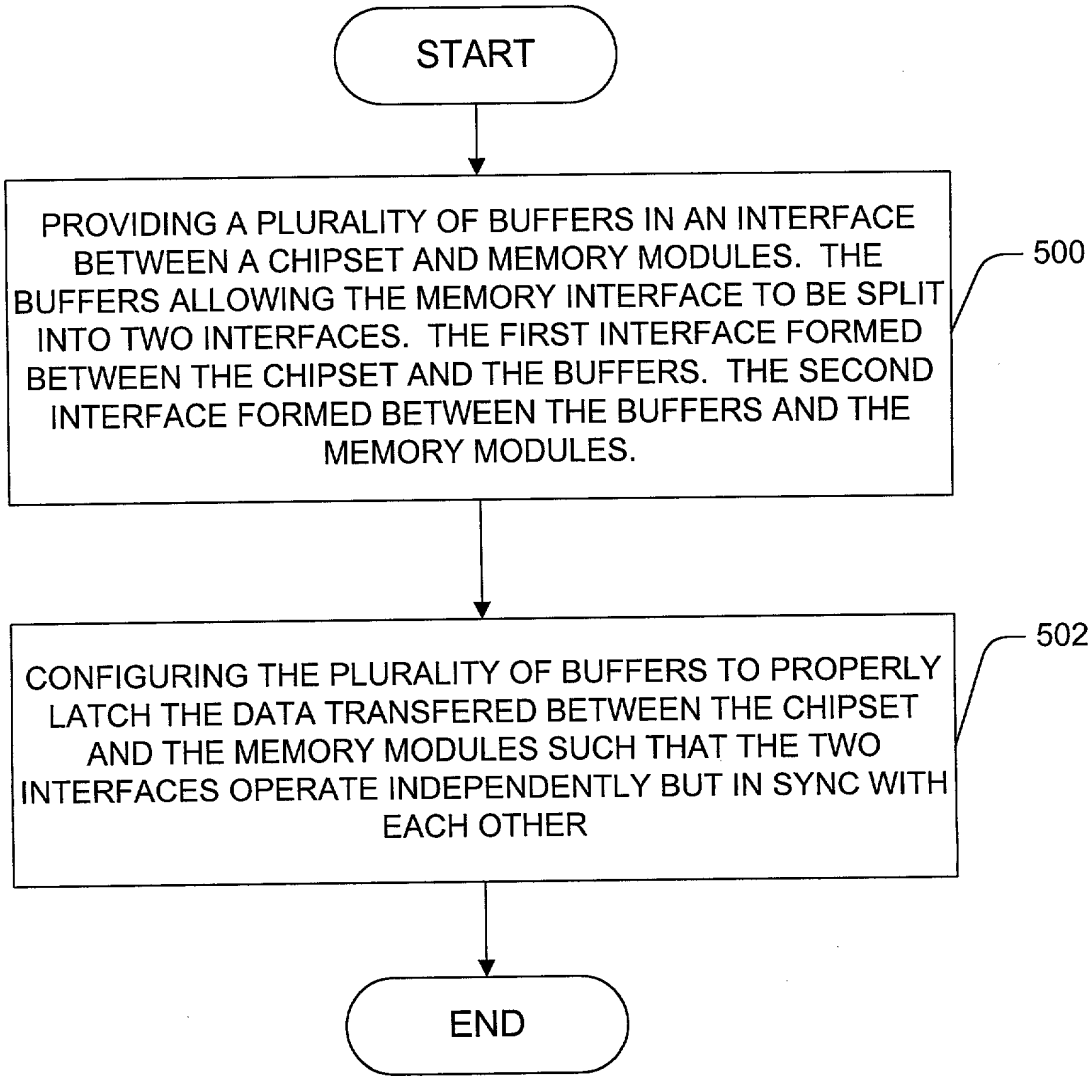
START
PROVIDING A PLURALITY OF BUFFERS IN AN INTERFACE BETWEEN A CHIPSET AND MEMORY MODULES. THE BUFFERS ALLOWING THE MEMORY INTERFACE TO BE SPLIT INTO TWO INTERFACES. THE FIRST INTERFACE FORMED BETWEEN THE CHIPSET AND THE BUFFERS. THE SECOND INTERFACE FORMED BETWEEN THE BUFFERS AND THE MEMORY MODULES.
500
CONFIGURING THE PLURALITY OF BUFFERS TO PROPERLY LATCH THE DATA TRANSFERED BETWEEN THE CHIPSET AND THE MEMORY MODULES SUCH THAT THE TWO INTERFACES OPERATE INDEPENDENTLY BUT IN SYNC WITH EACH OTHER
502
END

FIG. 5